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(54) Title: POWER DEVICES IN WIDE BANDGAP SEMICONDUCTOR

(57) Abstract

Described are preferred devices which include a semiconductor device such as a very high power switching device fabricated on a junction–isolated or semi–insulating substrate (e.g., silicon carbide).

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POWER DEVICES IN WIDE BANDGAP SEMICONDUCTOR

Background of the Invention

The present invention relates generally to semiconductor devices and in particular to high voltage/high power devices fabricated on semi-insulating substrates such as semi-insulating silicon carbide. For additional background information, including information pertaining to basic semiconductor device elements incorporated in devices of the present invention, reference can be made, for example, to U.S. Patents Nos. 5,448,081; 5,378,912; and 4,983,538, each of which is incorporated herein by reference in its entirety.

Summary of the Invention

One object of the present invention is to provide devices which allow blocking of very high voltages without the need for a very thick drift region which must be grown by epitaxy.

Another object of the present invention is to provide a lateral power device structure, such as a very high voltage (greater than 1000 v up to and greater than 10000 v) power switching device, fabricated on a junction-isolated or semi-insulating substrate in a wide bandgap semiconductor having a breakdown field substantially greater than silicon.

Another object of the present invention is to provide such lateral power devices in the form of a lateral metal oxide semiconductor field effect transistor (MOSFET) or lateral insulated gate bipolar transistor (IGBT) on silicon carbide.

Accordingly, one preferred embodiment of the invention provides a lateral power device structure fabricated in an epilayer (epitaxially-grown layer) on

a semi-insulating substrate, especially a semi-insulating silicon carbide substrate. Such a semi-insulating substrate can be achieved, for instance, by doping, e.g., with vanadium or similar dopant materials. The preferred devices include a semi-insulating silicon carbide substrate, and an epitaxially grown drift region (e.g., N-) adjacent the semi-insulating substrate (e.g., doped at a level of about 2-5 x 10^{15} cm^{-3}). A lateral semiconductor device, e.g., an insulated gate field effect transistor (or MOSFET) or IGBT is provided in the epilayer. Such devices include generally source and drain regions (e.g., both N+), an insulating layer (e.g., SiO_2), and a gate, e.g., formed of polysilicon. Other conventional semiconductor device features can also be included, as those skilled in the art will appreciate.

Additional objects, embodiments, and features of the invention will be apparent from the following description, and the drawings appended hereto.

Brief Description of the Drawings

Figure 1 shows a preferred lateral power device of the present invention.

Figure 2 shows depletion edges for several blocking voltages in an illustrative lateral power device of the present invention.

Description of the Preferred Embodiment

For the purposes of promoting an understanding of the principles of the invention, reference will now be made to certain preferred embodiments thereof and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, such alterations, modifications, and further applications of

the principles of the invention being contemplated as would normally occur to one skilled in the art to which the invention pertains.

Figure 1 shows a preferred lateral power device 11 of the present invention. Device 11 includes a semi-insulating layer 12, e.g., a semi-insulating silicon carbide substrate. Adjacent to layer 12 is an epitaxially-grown layer providing drift region 13 (e.g., N-). Drift region 13 may be doped, for example, at a level of about 2-5 x 10^{15} at/cm^{-3}, and may have a thickness of up to about 15 μM, e.g., about 10 to about 15 μm. Provided within layer 13 are source and drain regions 14 and 15 (which of opposite character to drift region 13, e.g., in the illustrated device N+; or, to provide an IGBT, drain region 15 can be P+), and a channel region 16. Also provided in device 11 is an insulating layer 17 (e.g., SiO_2) covering the channel region 16, and a gate 18 adjacent the insulating layer 17, for example formed with polysilicon (doped). Additional features may also be included in the device, for example conductive materials such as metal(s) to provide leads at the source and drain.

In an illustrative device such as that illustrated in Figure 1, in the off, or blocking condition, the PN-junction will extend a depletion region about 56 μm into the N- region before avalanche breakdown occurs (assuming a doping of 2 x 10^{15} cm^{-3}). This would correspond to a drain voltage of V=Emax/2 V_d = 5600v. Lateral structures in accordance with the preferred devices of the invention are particularly advantageous, since silicon carbide wafers with epilayers of about 10-15 μm are currently readily available commercially.

In the present invention, the semi-insulating substrate ensures that the substrate does not act as an equipotential boundary under the depleted drift region, which would confine the extent of the electric field to the regions under the base (P) region and under the drain (N+) region. Shown in Figure 2 are approximate depletion edges for several blocking voltages in an illustrative device of the present invention.

While the invention has been illustrated and described in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiment has been shown and described and that all changes and modifications that come within the spirit of the invention are desired to be protected.

CLAIMS:

1. A power switching device, comprising:

a semi-insulating substrate;

an epitaxially-grown layer adjacent said semi-insulating substrate providing a drift region;

source, drain and channel regions;

an insulating layer over said channel region; and

a gate adjacent said insulating layer.

2. The device of Claim 1, which is a transistor.

3. The device of Claim 2,which is an insulated gate field effect transistor.

4. The device of Claim 2, which is an insulated gate bipolar transistor.

5. The device of Claim 1, wherein the source and drain are N+, the channel is P, and the drift region is N-.

6. The device of Claim 1, wherein the semi-insulating substrate is silicon carbide.

7. The device of Claim 6, wherein the semi-insulating substrate is doped with vanadium.

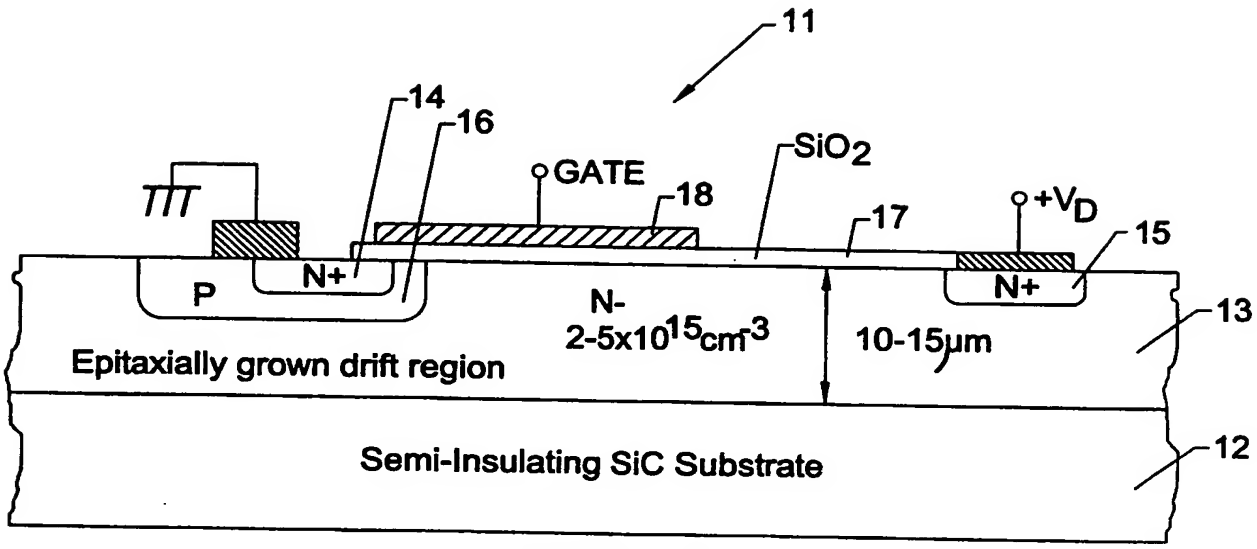

FIG. 1.

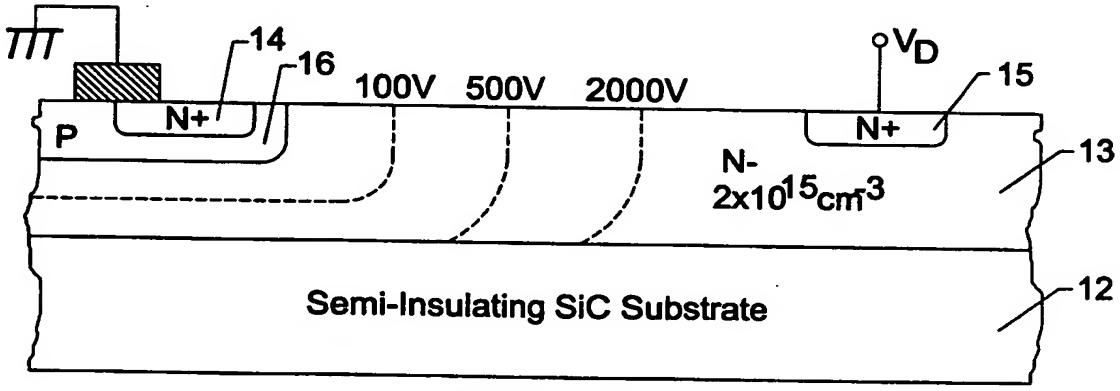

FIG. 2.

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(74) Agent: SUMMA, Philip; Suite 500, 5925 Carnegie Boulevard, Charlotte, NC 28209 (US).

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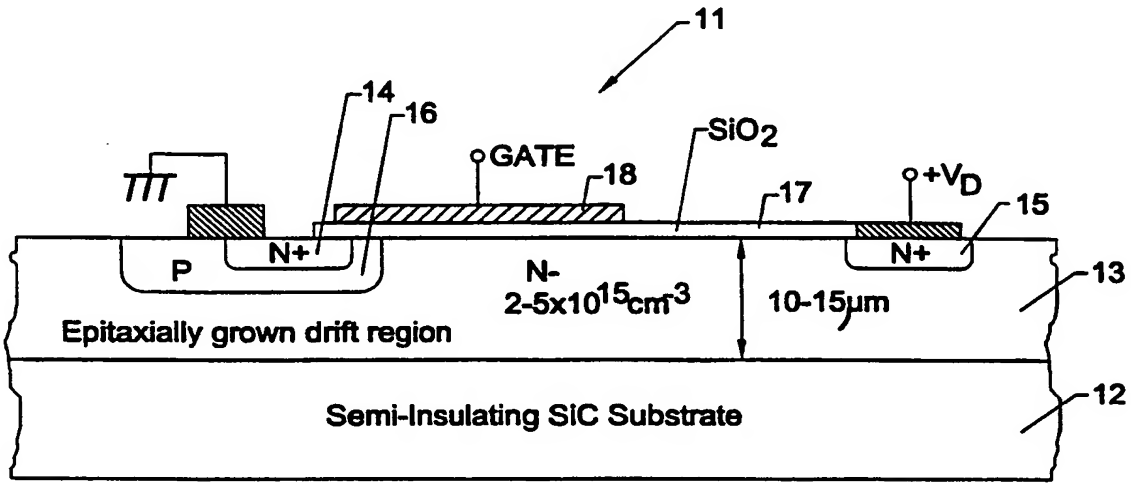

(57) Abstract

An insulated gate power semiconductor switching device (11) such as a lateral DMOSFET or a lateral IGBT disposed on a semi-insulating substrate (12). In particular, the substrate may consist of semi-insulating silicon carbide, eg. vanadium-doped SiC. Accordingly, high voltage lateral field-effect can be manufactured using readily available silicon carbide wafers having epilayers of about 10-15 micrometers.

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	US 5 378 912 A (PEIN H B) 3 January 1995 cited in the application	4
A	see column 3, line 10 - line 17; figures 1-3 see column 4, line 5 - line 25 see column 5, line 4 - line 35	1-3,5
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Date of the actual completion of the international search	Date of mailing of the international search report
15 December 1998	29/12/1998

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